Responsive to the objection to the disclosure based on informalities, Applicants have amended page 13, line 1, keeping in mind the comments offered by the Examiner. Applicants submit that the disclosure is now in allowable form and request that the objection to the disclosure be withdrawn.

Responsive to the objection to claims 2, 5, and 11 based upon informalities, Applicants have amended claims 2, 5, and 11, keeping in mind the comments offered by the Examiner. Applicants submit that claims 2, 5, and 11 are in allowable form and respectfully request that the objection to such claims be withdrawn.

Responsive to the rejection of claims 1-11 under 35 U.S.C. §112, 2nd paragraph, Applicants have amended claims 1 and 2, keeping in mind the comments offered by the Examiner. With respect to the variability of the gap as set forth at claim 1, lines 9 and 10, and claim 2, lines 12 and 13, such variability is consistent with the specification, e.g., page 9, the paragraph beginning at line 7 thereof. Specifically, cylinder 107 can be lowered to create a gap between cylinder 107 and the vacuum vessel top plate 103. For all the foregoing reasons, Applicants submit that claims 1-11 are now in allowable form and hereby respectfully request that the rejection thereof under 35 U.S.C. §112, 2nd paragraph, be withdrawn.

Responsive to the rejection of claims 1-4 and 6-10 under 35 U.S.C. §103(a) as being unpatentable over U.S. Patent No. 5,580,420 (Watanabe et al) in view of U.S. Patent No. 5,314,574 (Takahashi), Applicants have amended claims 1 and 2 and submit that claims 1-4 and 6-10 are now in condition for allowance.

Claim 1, as amended, recites in part:

> "...substrate stage having a substantially constant vertical position..."

Applicants submit that such an invention is neither taught, disclosed, nor suggested by any of the cited references, alone or in combination.

Watanabe et al disclose a wafer supplying system for supplying wafers to the substrate stage 148 and the lower vessel 48 below the process chamber 6. As the process chamber 6 and the substrate stage 148 are located on different planes in a vertical direction, there is a need to equip a mechanism for moving a substrate stage 148 up and down. Consequently, such a configuration of Watanabe et al results in poor maintainability because of the degree of congestion on the lower face of the apparatus. Additionally, the configuration of Watanabe et al presents another problem of shortening the lifetime of the wafer stage and so forth because of the lifting/lowering of the wafer temperature control mechanism, wafer electrostatic control mechanism, high frequency impression mechanism, wafer lifting mechanism, and the like together with the lifting/lowering of the wafer stage. Therefore, Watanabe et al fail to teach or suggest the invention as set forth in claim 1, as amended.

Takahashi discloses that the loading platform 18 is arranged atop intermediate cover 19. A raising and lowering mechanism, for example an inner cylinder 24, is provided for raising and lowering intermediate cover 19. As seen from Figs. 1 and 6, both loading platform 18 and intermediate cover 19 are together raised and lowered by actuation of air cylinder 24, thereby also raising and lowering

semiconductor wafer W. Therefore, Takahashi fails to teach or disclose the invention as set forth in claim 1, as amended.

On the other hand, the present invention has various advantages associated therewith. The wafer stage is fixed in the process chamber such that the gate valve is not required for assuring the axial symmetry with respect to the wafer arrangement in the process chamber. As the gate valve is not used, the floor occupation space of the cluster tool will be about 1/3 of the conventional cluster tool. Further, as the mechanism for moving the wafer stage up and down is not required, a wide space under the lower face of the apparatus can be obtained. Therefore, the present invention results in excellent maintainability. It is noted that each of the cited references does not disclose or teach any such advantage.

For all the foregoing reasons, Applicants submit that claims 1-4 and 6-10 are in condition for allowance and respectfully request that the rejection of claims 1-4 and 6-10 under 35 U.S.C. §103(a) be withdrawn.

In a similar manner, claim 2 recites in part:

> "...each of said substrate stages having a substantially constant vertical position..."

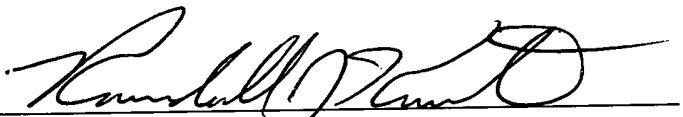
Applicants submit that claim 2, which sets forth subject matter substantially similar to that set forth with respect to claim 1 above, is thus also in condition for allowance for reasons similar to those given for claim 1, above.

Claims 5 and 11 are rejected under 35 U.S.C. §103(a) as being unpatentable over Takahashi, as applied to claims 1-4 and 6-10 above, and further in view of JP10-177994(Nasahiro et al). However, claims 5

and 11 each depend from claims 1, which is in condition for allowance for the reasons set forth above. Thus, Applicants submit that claims 1 and 5 are in condition for allowance and hereby respectfully request that the rejection thereof under 35 U.S.C. §103(a) be withdrawn.

If the Examiner has any questions or comments that would speed prosecution of this case, the Examiner is invited to call the undersigned at 260/485-6001.

Respectfully submitted,



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RJK/ste10

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Replacement Claims
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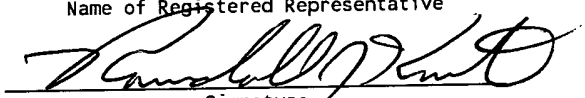

Signature
October 1, 2002
Date

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other parts are similar to Fig. 4 and Fig. 5.

The shower plate 303 is composed of dielectric material. The radial slot line antenna 301 is supplied with microwave from coaxial wave-guide 304. Microwave radiated from the radial line slot antenna 301 is introduced into the processing chamber through the dielectric plate 302 and the shower plate 303, and this micro wave creates plasma in the processing chamber. In the processing chamber, plasma etching, resist ashing, plasma CVD (chemical vapor deposition) or other processing can be performed on the wafer.

(Embodiment 4)

Fig. 7 and Fig. 8 are schematic cross-section views showing an example of the semiconductor manufacturing apparatus according to the present invention. Fig. 7 shows the section A-A' of Fig. 8 and Fig. 8 the section B-O-B' of Fig. 7. In the vacuum vessel, only a part including the processing chamber is shown. 401 designates permanent magnet, 402 wafer, 403 electrode and 404 high frequency power source. The other portions are similar to the example of fig. 4 and Fig. 5. In this example, permanent magnet is not disposed near the wafer transport path and near its opposite angle portion. However, a permanent magnet may be disposed near the opposite angle portion near the wafer transport path.

A plurality of permanent magnets 401 is disposed substantially on the circumference, in order to impress magnetic field around the wafer. High frequency impression to the electrode 403 by the high

frequency source 404 generates plasma in the processing chamber. Magnetic [filed] field impression improves the plasma generation efficiency to enable to generate a high-density plasma. For instance, 13.56 MHz is adopted as high frequency and 120 Guass as magnetic flux density around the wafer. In the processing chamber, plasma etching, resist ashing, plasma CVD (chemical vapor deposition), sputter film deposition or other processing can be performed on the wafer.

(Embodiment 5)

Fig. 9 to Fig. 11 are schematic cross-section views showing an example of the semiconductor manufacturing apparatus according to the present invention. Fig. 9 Shows the section A-A' of Fig 10 or Fig. 11 and Fig. 10 or Fig. 11 the section B-O-B' of Fig 9. In the vacuum vessel, only a part including the processing chamber is shown. 501 designates upper permanent magnet, 502 lower permanent magnet, and 503 lower permanent magnet in the transport chamber. In this example, permanent magnets are disposed near the wafer transport path and also near its opposite angle portion. The other portions are similar to the example of Fig. 7 and Fig. 8. Respective permanent magnets 501, 502, and 503 are disposed in the position not interfacing with the wafer transport. In the example of Fig. 10, the lower permanent magnet 502 is installed in the atmosphere, while in the example of Fig. 11, the lower permanent magnet 503 is installed in the transport chamber. As the permanent magnets are installed also near the wafer

MARKED-UP CLAIMS

Please amend claim 3 as follows:

3. The semiconductor manufacturing apparatus according to Claim 1 [or 2], wherein said vacuum vessel can be divided into a part including said processing chamber and a part having said substrate transport mechanism.

Please amend claim 4 as follows:

4. The semiconductor manufacturing apparatus according to Claim 1, [and Claim 3] further comprising a plasma generation mechanism for generating plasma in said processing chamber.

Please amend claim 5 as follows:

5. The semiconductor manufacturing apparatus according to Claim 4, wherein said plasma generation mechanism radiates microwave [thorough] energy through a slot antenna.